Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

UG/PG DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2026

Second Semester

Applied Electronics

PAPE2408 - VLSI DESIGN TECHNIQUES

Regulations - 2024

Duration: 3 Hrs ***Maximum: 100 Marks***

PART – A(ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Define Threshold voltage in CMOS	L1	1	2
2.	What are the two types of Layout design rules?	L1	1	2
3.	Define transistor sizing.	L1	2	2
4.	List the various modeling in Verilog.	L1	2	2
5.	Which MOS can pass logic1 and logic 0 strongly?	L1	3	2
6.	List the functions of synchronizer.	L1	3	2
7.	Compare functionality test and manufacturing test.	L2	4	2
8.	What is design for feasilbility	L1	4	2
9.	Contrast tasks and functions.	L2	5	2
10.	Recall the two basic statements in behavioural modelling.	L1	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	Describe the idea I-V characteristics of CMOS invertor with suitable sketches	L2	1	16
		Or			
	b	Explain the DC transfer characteristics of CMOS invertor with neat sketches	L2	1	16
12.	a	i Explain in detail about power dissipation.	L2	2	8
		ii Explain how to estimate the delay in a MOSFET	L2	2	8
		Or			
	b	Write Verilog code for a full adder using various types of modeling with a suitable diagram	L2	2	16
13.	a	Compare two-phase latch max-delay constraint and flip-flop min-delay constraint with their characteristics	L4	3	16
		Or			
	b	Compare the circuit design of latches and flip flops and analyze their characteristics.	L4	3	16
14.	a	Identify how logic verification is done in a circuit with a flow diagram.	L2	4	16
		Or			
	b	Explain the concept of boundary scan testing for digital circuits	L2	4	16
15.	a	Explain the concept involved in Timing control in Verilog.	L2	5	16
		Or			
	b	Illustrate the concept of gate delay in Verilog with example	L2	5	16

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